Analysis of Flexible Design Options for Mixed-Signal Integrated Circuit Products

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IDS.332 FINAL REPORT

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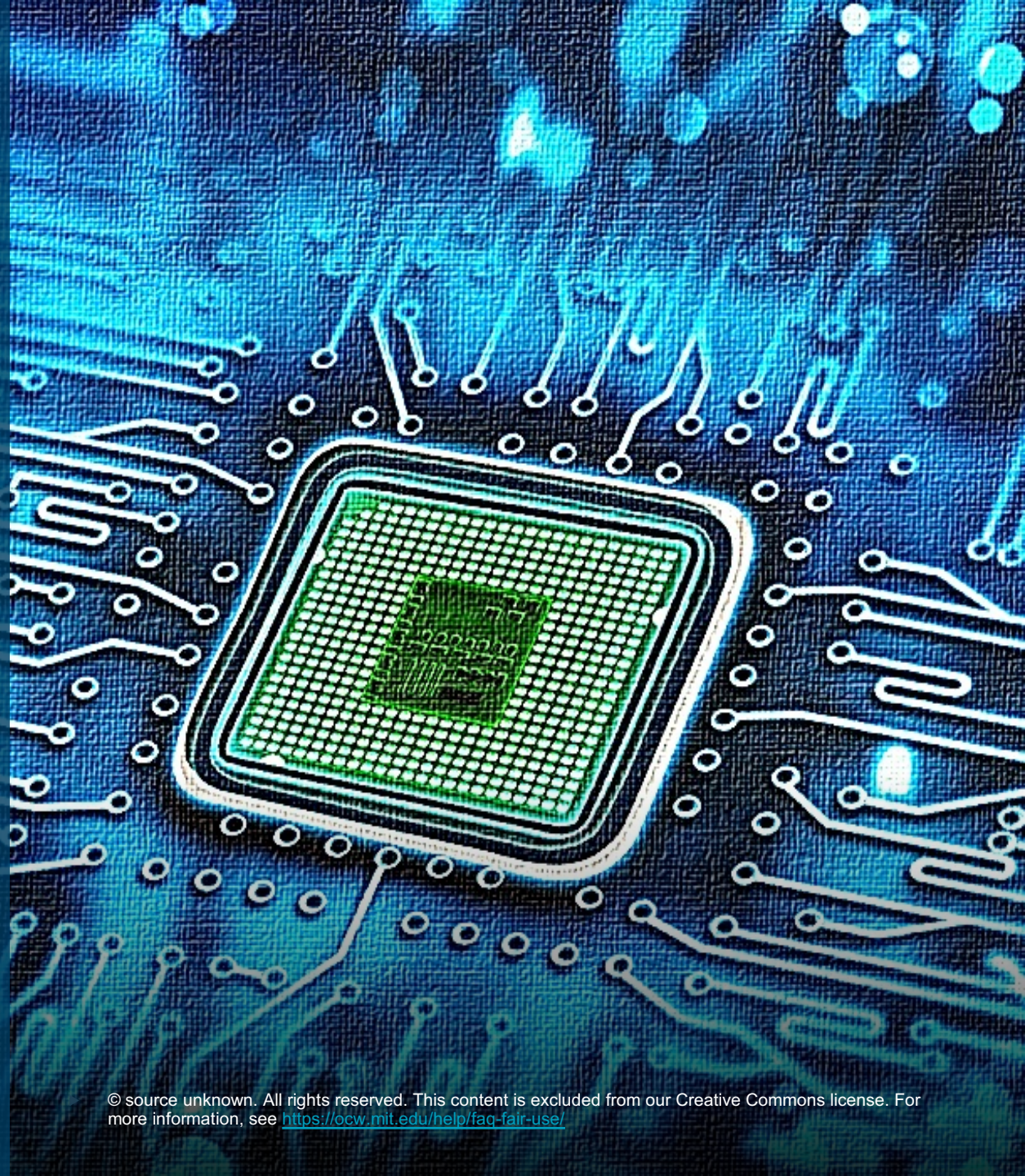
12/12/2017

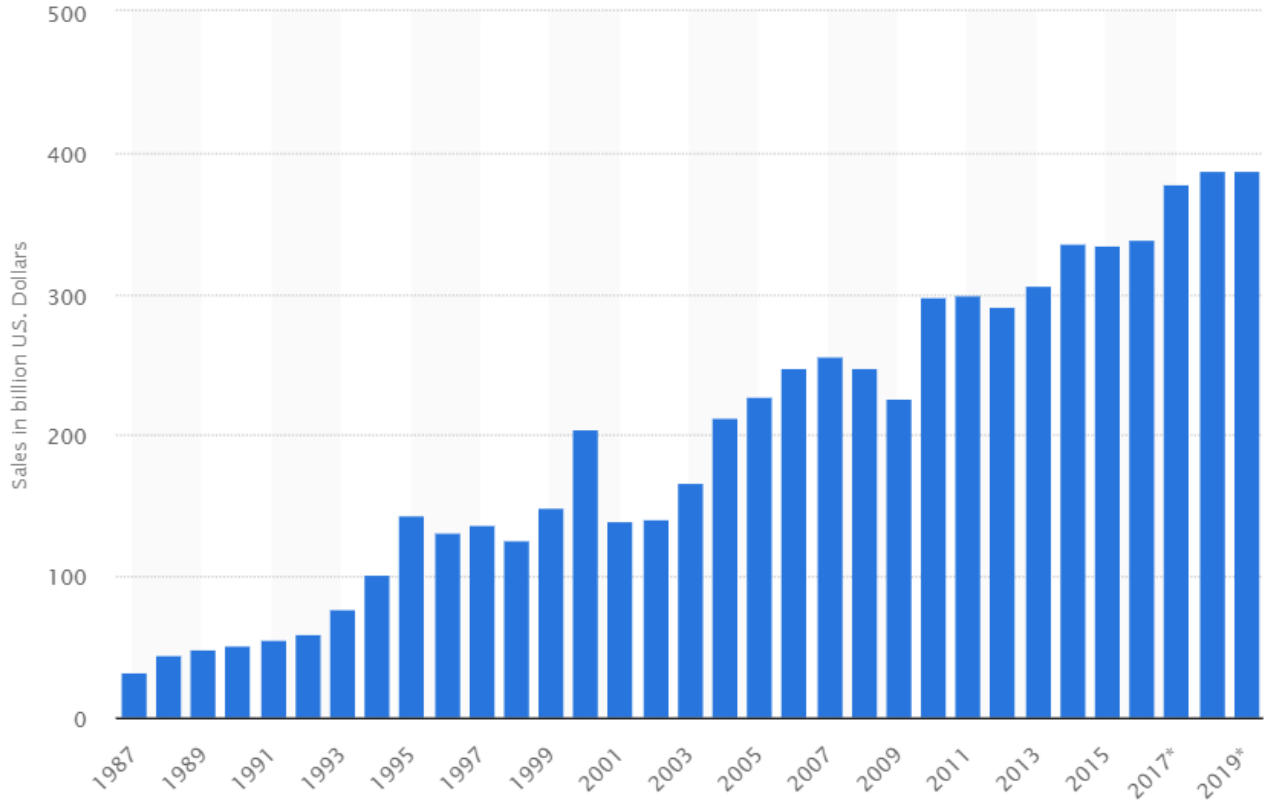


Agenda

- Background
- Problem Statement
- Analysis Approach
- Recommended Strategy
- Questions

Background: Semiconductor Industry

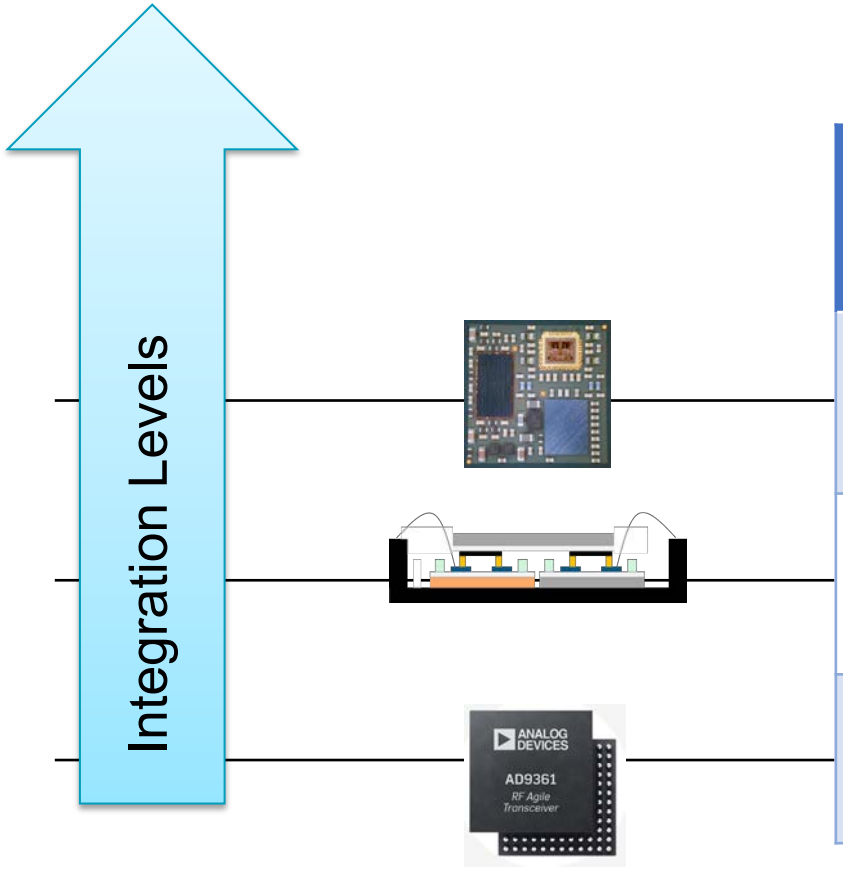
- **$378 Billion Industry**
- **Expected to grow 12%** in 2017
- Historically, driven by **Economy of Scale** (EoS) **benefits** associated with **Moore's law**
- Recent years have focused on **energy-efficiency rather than speed**
- Due to the capital investment required, **companies are re-thinking their plans in fine-line geometries**



Additional Information
World; World Semiconductor Trade Statistics; 2017

Sources
WSTS; SIA

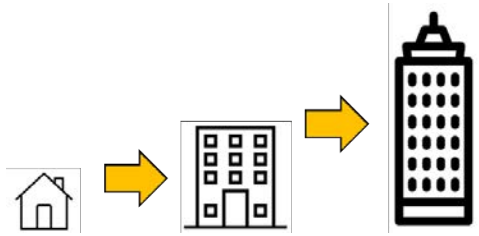
Background:
IC Integration Levels



Integration Type	IC Process	IC Die	Package(s)	Resistors, Inductors, Capacitors (RLC)
System in Package (SiP)	1 or more	2 or more	1	Few (optional)
Heterogeneous (Hetero)	2 or more	1 or more	1	None
Monolithic (Mono)	1	1	1	None

Introduction:
Economy of Scale (EoS) Benefits in Monolithic Integration

EoS compels companies to:



- **Build Big**
  - To overcome initial Non-Recurring Engineering (NRE) costs
  - Compels companies to integrate super-set of all target customer's functionality demands

- **Commit Early**
  - To reduce mask sets
  - Customer configurations must be known in advance and included in the initial design

- **Couple Developments**
  - All functionality must be finished prior to mask set creation
  - Exposes companies to competitive threats since customers cannot see actual working silicon until all developments complete

Introduction:
Monolithic Integration Challenges

Building Big, Committing Early, and Coupling Developments:

- Creates all-or-nothing dependencies
- Increases the project risk under uncertainty
- Hinders the project from quickly responding to future customer future needs
- Increases dependent complexity

Problem Statement

To maximize the Net Present Value (NPV) of a mixed-signal Integrated Circuit (IC) product

By creating a flexible development strategy in the face of uncertainty*

Using decision rules to modify System in Package contents as demand changes

*uncertain product demand,

*uncertain project costs, and

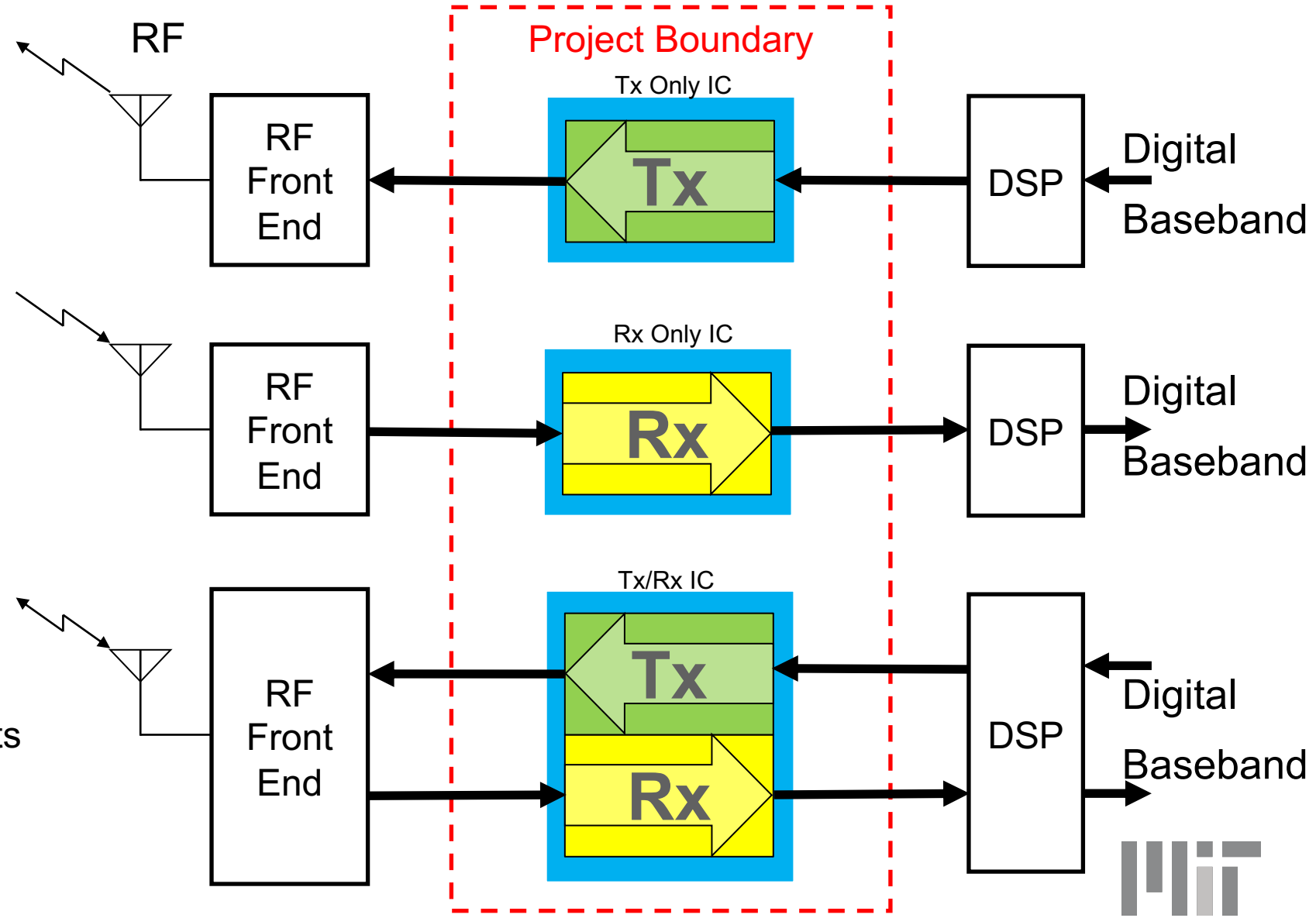
*uncertain project execution timelines

Target Applications

1) Transmit (Tx) Only Products

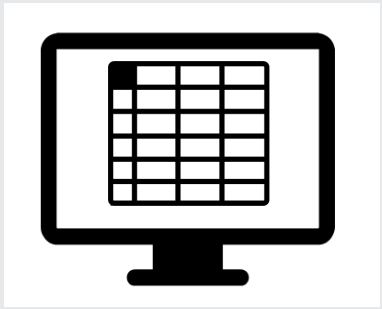
2) Receive (Rx) Only Products

3) Transceiver (Tx and Rx) Products



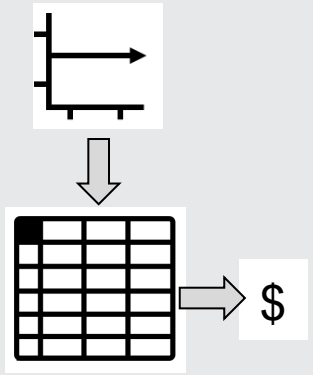
Analysis Steps

Step 1



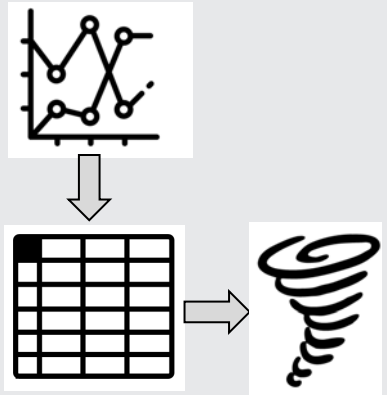
Develop NPV valuation model of Mono & SiP Integration for IC Products

Step 2



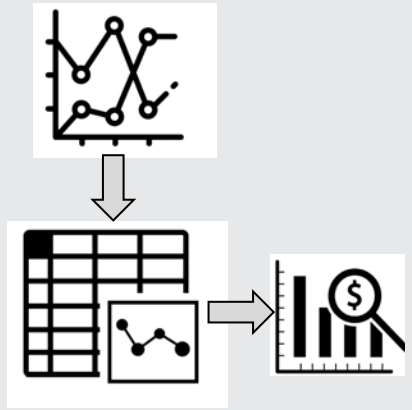
Calculate Deterministic NPV for Mono Integration using Static Inputs

Step 3



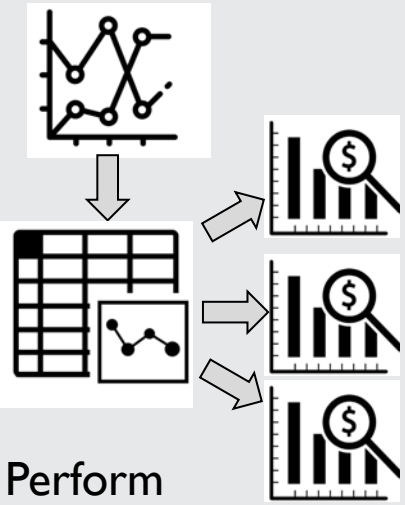
Perform Sensitivity Analysis on NPV Model (Tornado Diagram)

Step 4



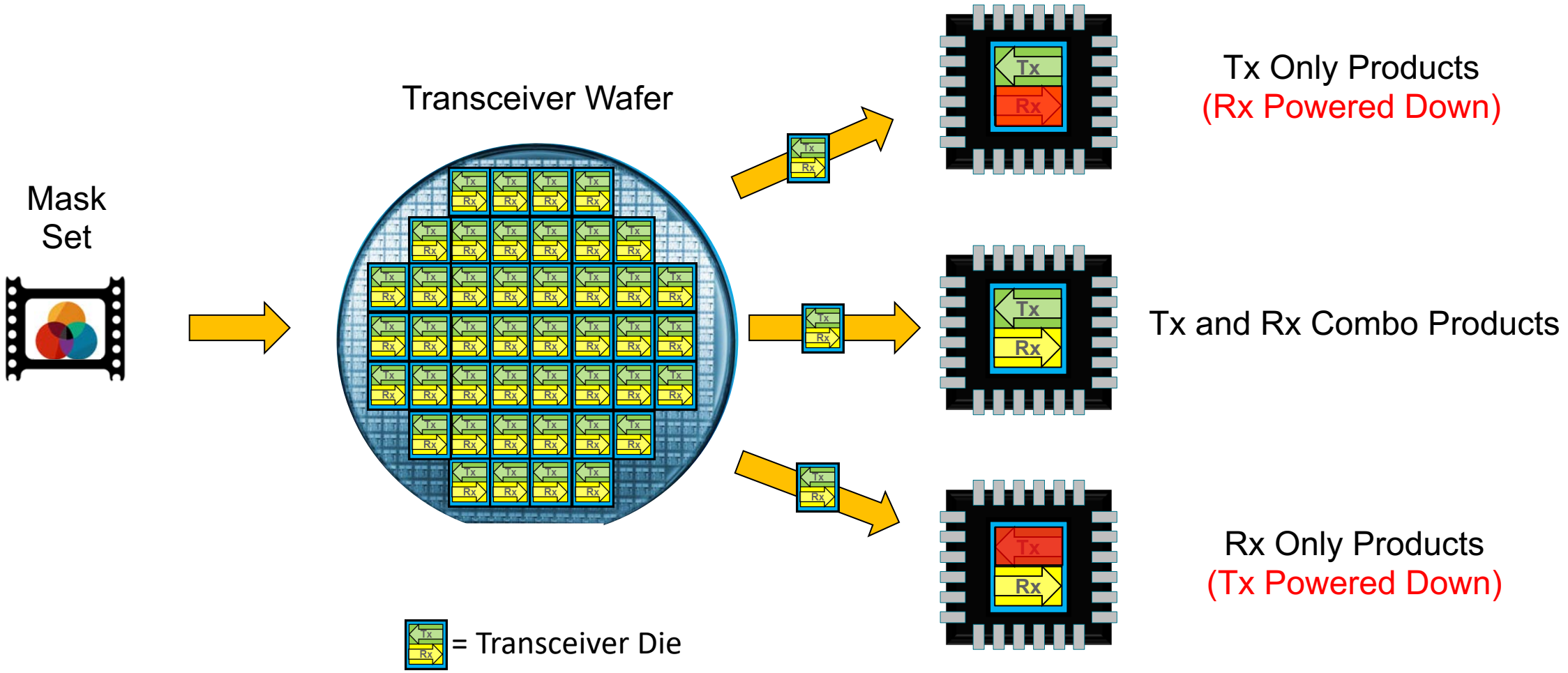
Perform Probabilistic NPV Analysis on Mono Integration using Monte Carlo (n=2000)

Step 5

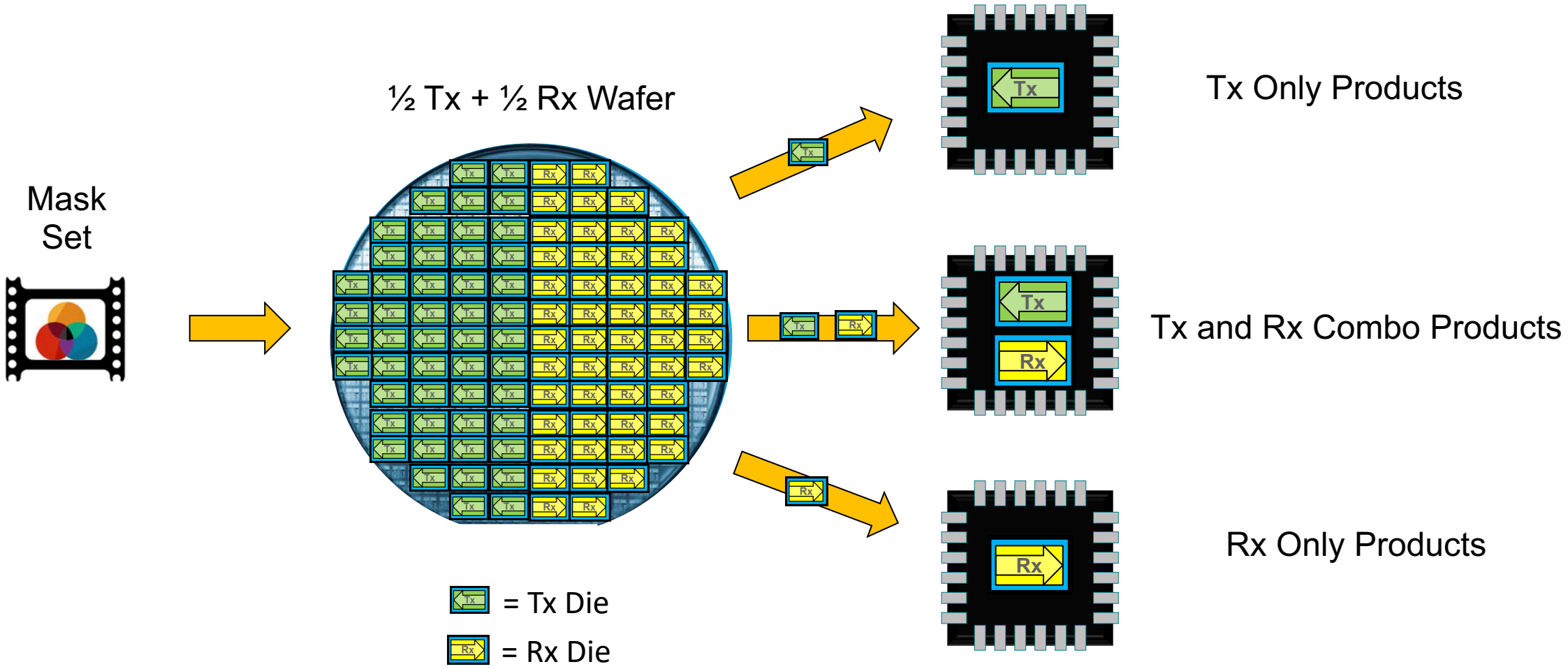


Perform Probabilistic NPV Analysis on Mono & SiP Integration using Monte Carlo (n=2000)

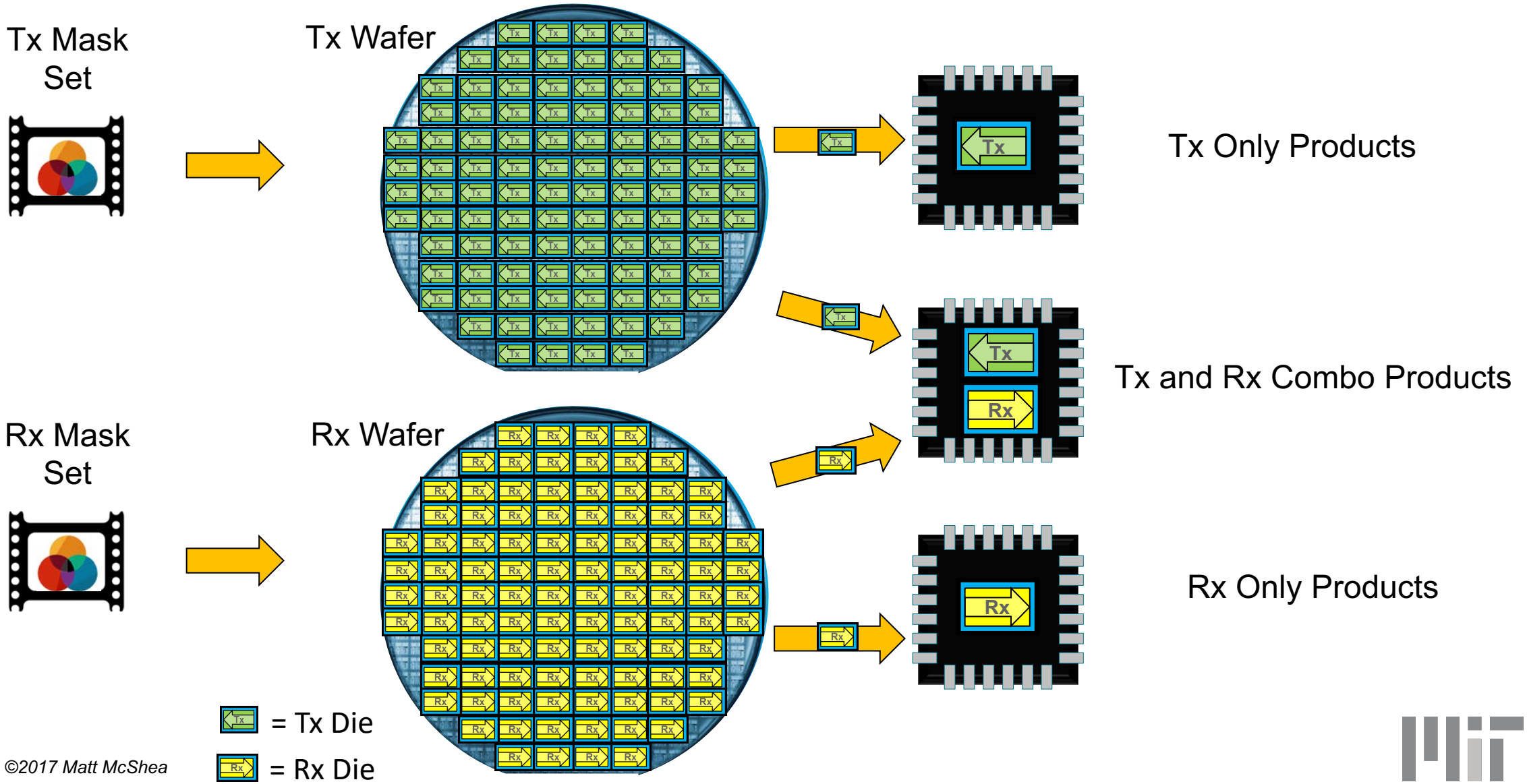
Base Case + Flexible Option #1
Monolithic Integration (One Mask – One Die)



Flexible Option #2
System in Package Integration (One Mask – Two Die)



Flexible Option #3
System in Package Integration (Two Mask - Two Die)

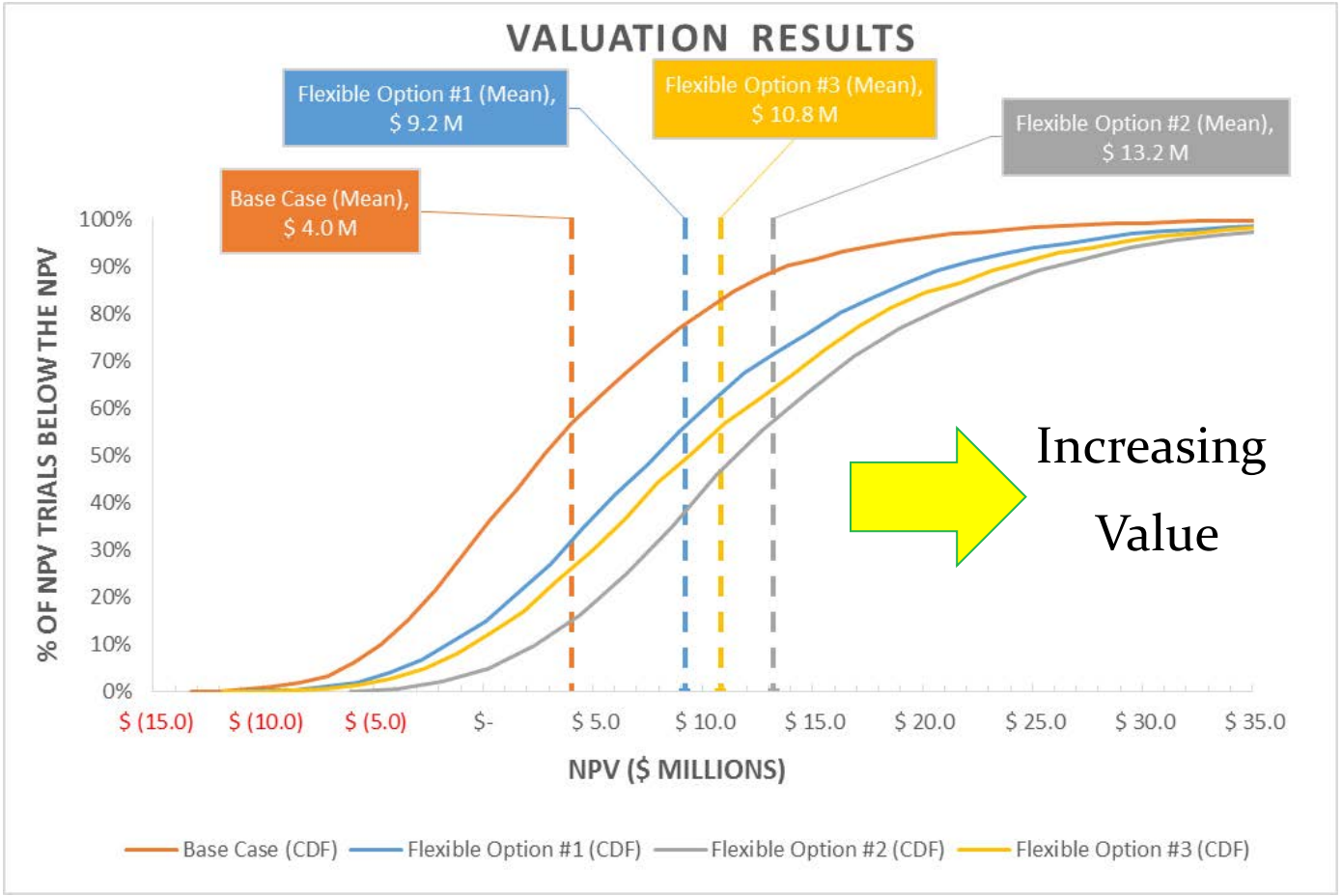


Comparison Parameters

Parameter	Base Case	Flexible Option #1	Flexible Option #2	Flexible Option #3
Integration Type	Mono	Mono	SiP	SiP
# Mask Sets	One	One	One	Two
# Die	One	One	Two(Tx,Rx)	Two(Tx,Rx)
Capacity Assumptions	Static	Dynamic	Dynamic	Dynamic
Capacity Dependency	None	None	Tx=Rx	None
Schedule Dependency (Tx)	max(Tx,Rx)	max(Tx,Rx)	max(Tx,Rx)	Tx
Schedule Dependency (Rx)	max(Tx,Rx)	max(Tx,Rx)	max(Tx,Rx)	Rx
Cost Dependency (Tx)	Tx + Rx	Tx + Rx	Tx	Tx
Cost Dependency (Rx)	Tx + Rx	Tx + Rx	Rx	Rx

Monte Carlo Simulation (n=2000) Results

- Flexible Option #2 (SiP Integration w/ one mask, two die)
  - provided the highest average NPV value at **$13.2M**.
  - Improves the average NPV by $2.4M to $9M relative to the other options.
  - 90% probability that the NPV will lie between:
    - P5 = +$0.5 and
    - 95 = +$25.9 million,

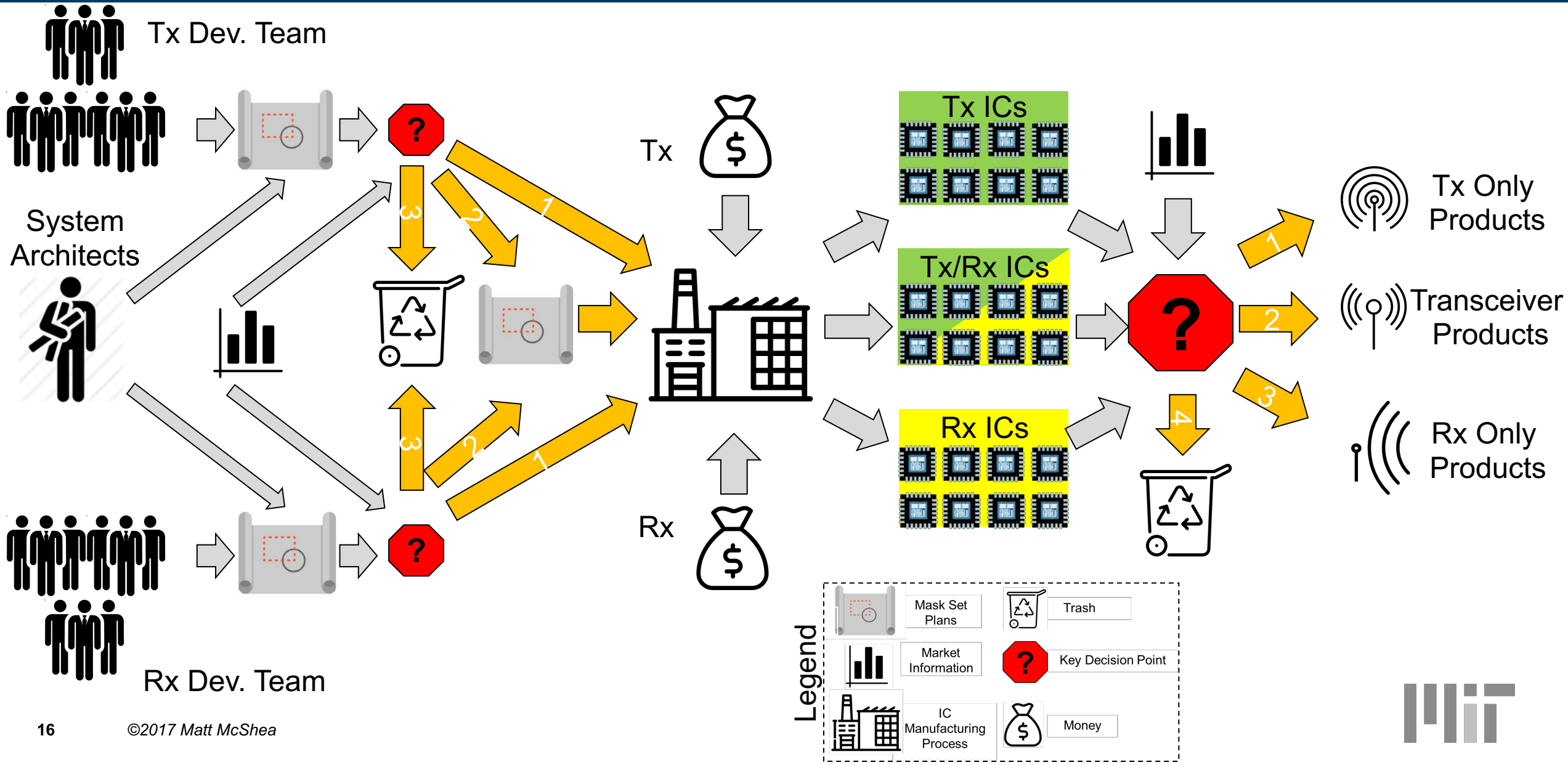


Results Summary

Evaluation Metrics	Base Case	Flexible Option #1	Flexible Option #2	Flexible Option #3
NPV (VaR_5) - 90% confidence min	-$8.9M	-$6.3M	**-$3.1M**	-$5.4M
NPV (VaR_{10}) - 80% confidence min	-$6.0M	-$2.9M	**$0.5M**	-$1.8M
NPV (mean)	$4.0M	$9.4M	**$13.2M**	$10.8M
NPV (VaG_{90}) - 80% confidence max	$14.1M	$21.2M	**$25.9M**	$23.4M
NPV (VaG_{95}) - 90% confidence max	$17.0M	$24.6M	**$29.5M**	$27.0M
NPV (std dev)	**$7.9M**	$9.6M	$10.1M	$10.0M
Flexibility Value (mean)	-	$5.5M	**$10.3M**	$7.5M
Fixed Cost (mean)	**$18.1M**	**$18.2M**	**$18.1M**	$22.3M
Fixed Cost (std dev)	$1.4M	$1.4M	$1.4M	$1.4M

*__Bold__ entries represent the best alternative between options

Recommended Decision Making Strategy:
SiP Integration w/ one or two mask, two die



Recommended Strategy

- **Hybrid approach between Flexible Option #2 and Flexible Option #3**
- Plan for two separate Tx and Rx die
- Defer decision on # of mask sets needed (one vs two), until Rx or Tx developments are close to completion
- If one development team finishes early, management can decide to either
  - Pay for two mask sets or
  - Wait for second development to finish and only pay for one mask set
  - Decision made at time when additional information would be known about the market demand.
- Minimizes the silicon cost for Tx and Rx Only applications – enables Tx/Rx Integration!

See previous slide for visual

Benefits of Recommended Flexible Strategy

- **<u>Increases Project Flexibility</u> due to Deferred Commitments**
  - Pushes integration decisions to later point in time – when more information available
  - Since customer demand dynamically changes over time:
    - **Flexible Approach Enables Future Expansion** – Allows new combinations of integrated products through laminate changes (simpler and cheaper to modify than silicon mask layers)
    - **Allows Performance Scaling** – With separate semiconductor die, opportunity to optimize functionality for RF, Analog or Digital content
- **Reduces Costs (Tx Only & Rx Only)**
  - Tx and Rx functionality exist on separate die which minimizes the full-factory cost of the silicon for Tx and Rx Only applications and improves the Gross Margin (GM) on those products.
- **Decouples Developments**
  - Each subsystem can be given its own die or even mask set
  - Subsystems developed independently
  - Reduces product development risk for Tx Only and Rx Only products (removes the all-or-nothing barrier)

Summary

- SiP Integration strategy
  - Provided the highest NPV (**$13.2M**)
  - Scored the best overall according to the evaluation metrics (**22% increase**)
  - Minimizes downside risk and maximizes upside opportunities
- Flexible SiP options:
  - Defer integration decisions, which…
  - Enables future expansion by…
  - Allowing new product configurations as market demand changes

    Resulting in….
  - **Increased Value**

Questions

References

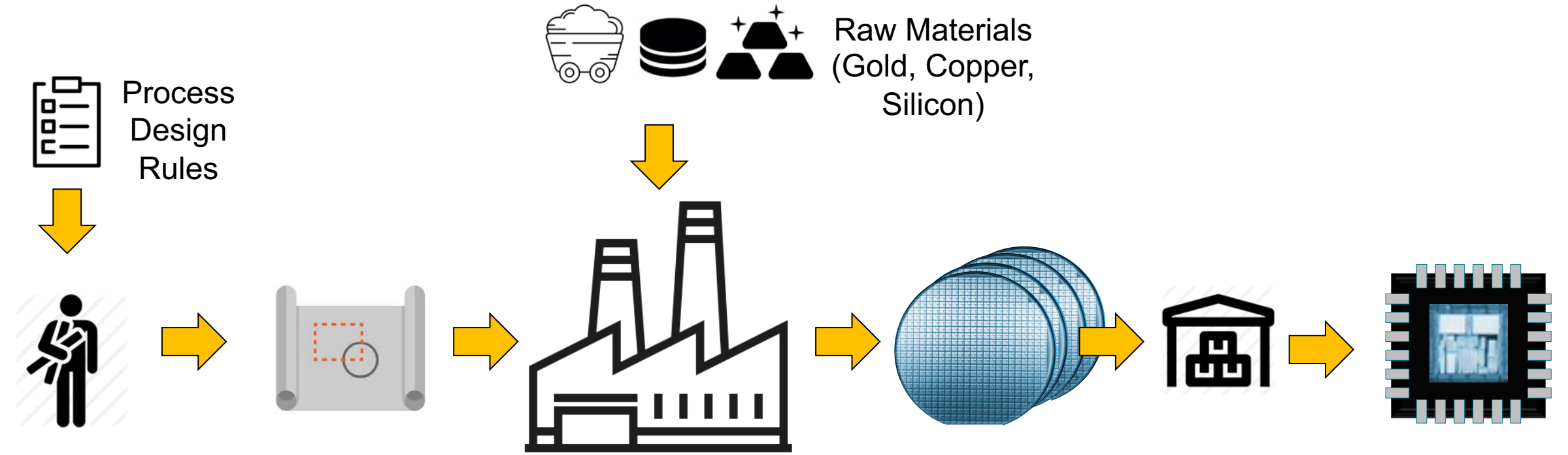
- [1] http://www.nasdaq.com/article/semiconductor-industry-outlook-april-2017-cm780023
- [2]https://www.semiconductors.org/news/2017/10/02/global_sales_report_2017/monthly_semiconductor_sales_reach_35_billion_globally_for_first_time_in_august/
- [3] https://www.statista.com/statistics/266973/global-semiconductor-sales-since-1988/
- [4] http://www.economist.com/technology-quarterly/2016-03-12/after-moores-law
- [5] MIT SDM 2016/17 Capstone Project – Analysis of IC System Integration Models and Their Market Viability - Gina Aquilano, Matt McShea, Wyatt Taylor
- [6] https://en.wikipedia.org/wiki/Semiconductor_device_fabrication
- [7] http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter2.pdf
- [8] https://ycharts.com/companies/ADI/gross_profit_margin
- [9] https://www.investopedia.com/terms/n/npv.asp
- [10] https://hbr.org/2014/11/a-refresher-on-net-present-value
- [11] Images:
  - IC image: http://news.mit.edu/2016/electron-phonon-interactions-affect-heat-dissipation-computer-chips-1012
  - Wafer Image: https://www.electronicsweekly.com/news/business/silicon-wafer-shipments-grow-8-2-year-2017-10/
  - Clipart Icons made by Freepik from www.flaticon.com
- [12] de Neufville, Richard. *Garage Case Template*. Excel Document. Accessed October 2017.
- [13] de Neufville, Richard and Stefan Scholtes. Flexibility in Engineering Design. MIT Press, 2011.

Backup Slides

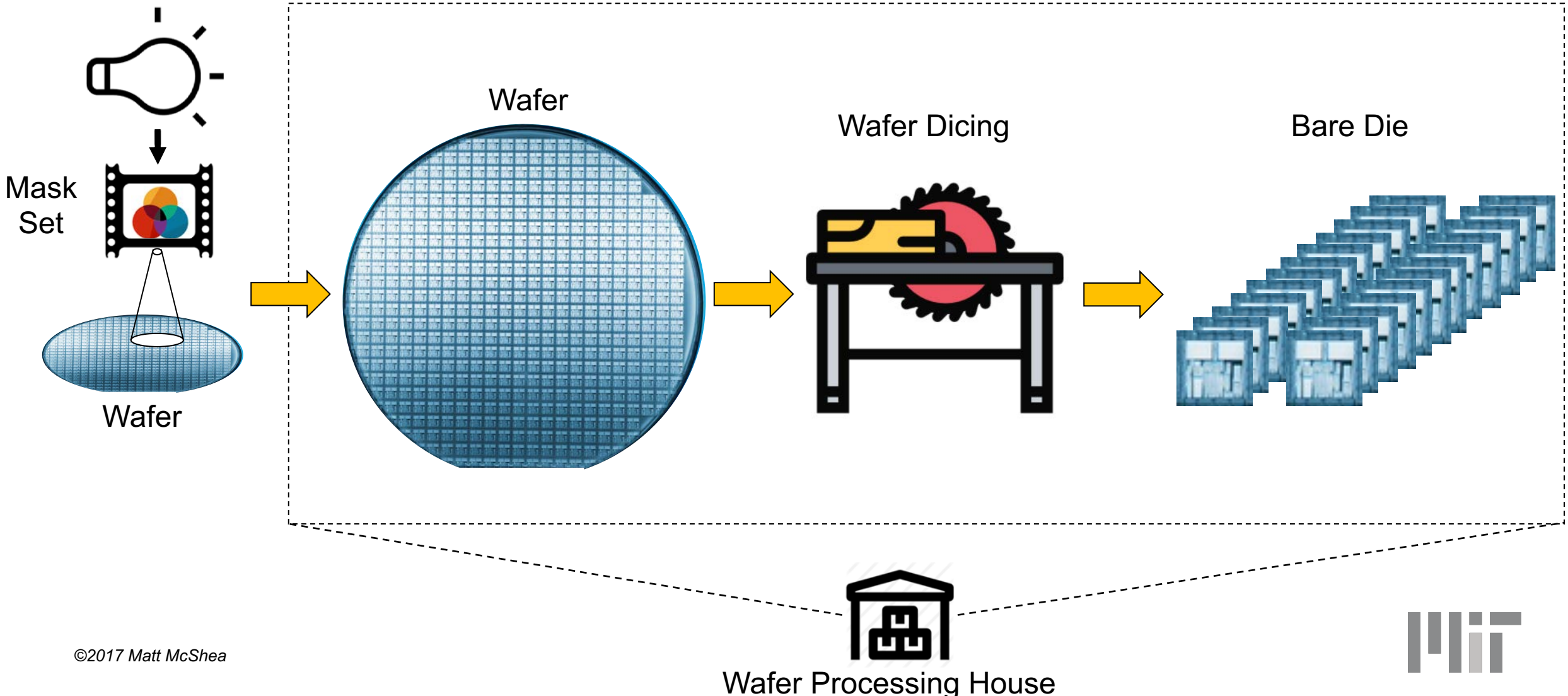
Implementation Barriers

Type	Barrier	Mitigation
Technical	Requires development of **slow chip-to-chip** data and control **interfaces** between Tx and Rx die.	**Planning ahead** to ensure buy-in by soliciting feedback from all relevant stakeholders, and creating a formal specification for these interfaces with the goal of handling at least 2 generations of products.
Management	**Future managers do not know about capability** to create new products from Tx or Rx die.	**Create an integrated product delivery team** which would collaborate between design and decision making teams.
Management	**Key managerial stakeholders** could **block** the **development** of Tx or Rx standalone die – or any developments which would prevent Monolithic transceiver development.	**Develop a long-term roadmap** outlining future transceiver products from the Tx and Rx die. This roadmap must include a game plan which is understood by the key managerial stakeholders.
Competitive	**External competitive pressure** forces the company to use Monolithic Integration to take advantage of the Economy of Scale benefits.	**Combine the Tx and Rx die into a single Monolithic die**. At the same time, continue to support the Tx and Rx die in the
Feasibility	Overhead associated with two die solution may require **replicated logic** (bias, calibrations, etc.) which would **affect the feasibility** of the SiP solution	During this investigation, the recommendations listed above hold, so long as the replicated logic does not represent >25% overhead on the two die SiP solution. **Ensure replicated logic does not represent >25% overhead.**

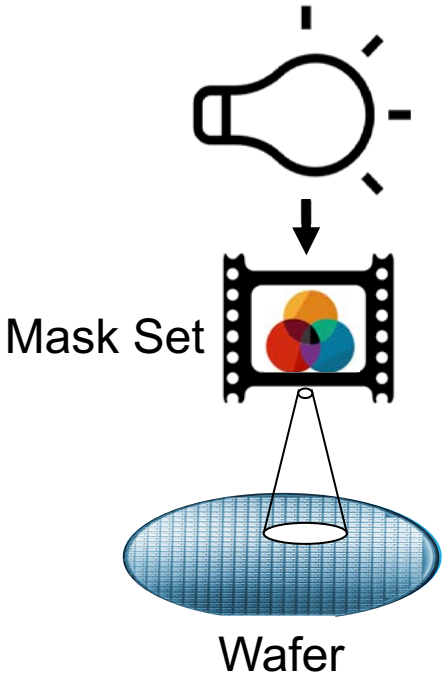
Background:
IC Manufacturing Process

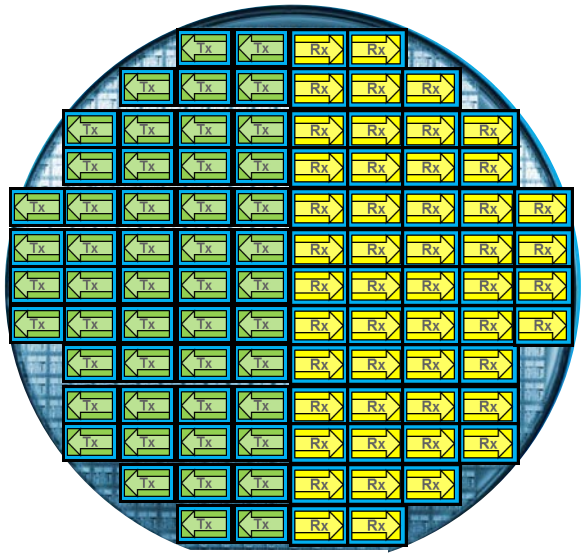


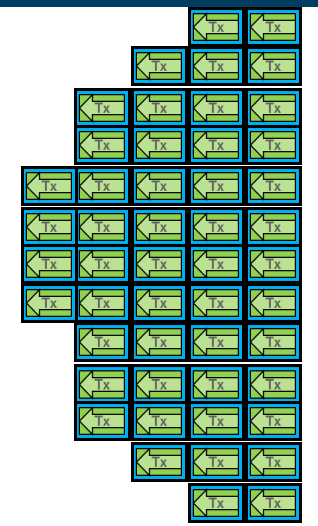
Wafer Processing (Generic)

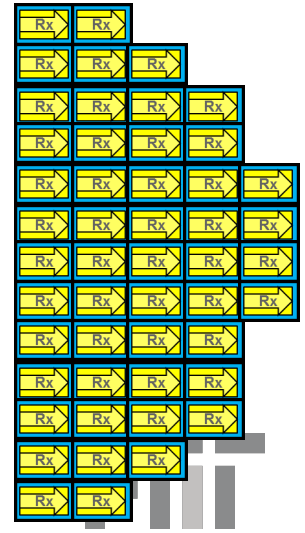


Wafer Processing (½ Tx + ½ Rx Wafer)









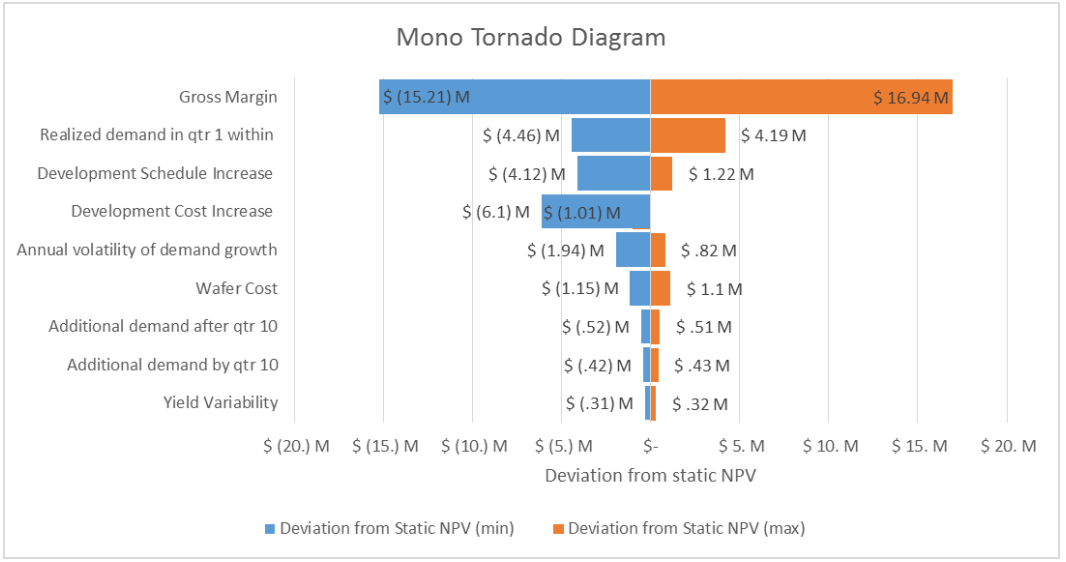
Model Uncertainty Assumptions

ID	Uncertainty	%	Comments
1	Realized demand in qtr 1 within	50%	+/- from projection
2	Additional demand by qtr 10	50%	+/- from projection
3	Additional demand after qtr 10	50%	+/- from projection
4	Annual volatility of demand growth	50%	of growth projection
5a	Development Schedule Increase (mean)	18%	normal dist. from projection
5b	Development Schedule Increase (std dev)	21%	
6a	Development Cost Increase (mean)	39%	normal dist. from projection
6b	Development Cost Increase (std dev)	20%	
7a	Gross Margin (mean)	0%	normal dist. from projection
7b	Gross Margin (std dev)	5%	
8	Wafer Cost	10%	+/- from projection
9	Yield Variability	2.5%	+/- from projection

Model Sensitivity

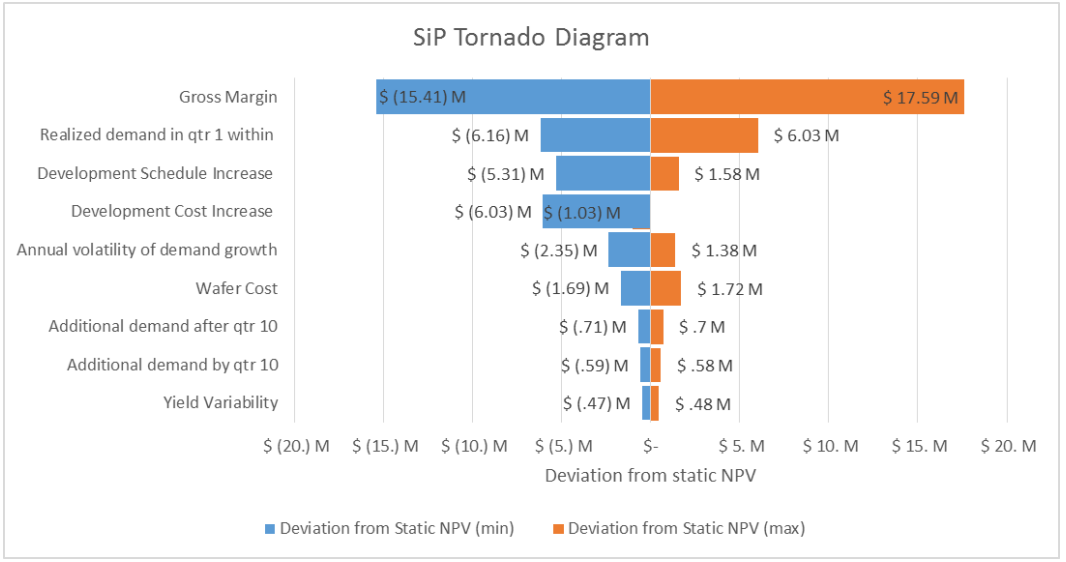
Monolithic Integration

Deterministic NPV = $9M

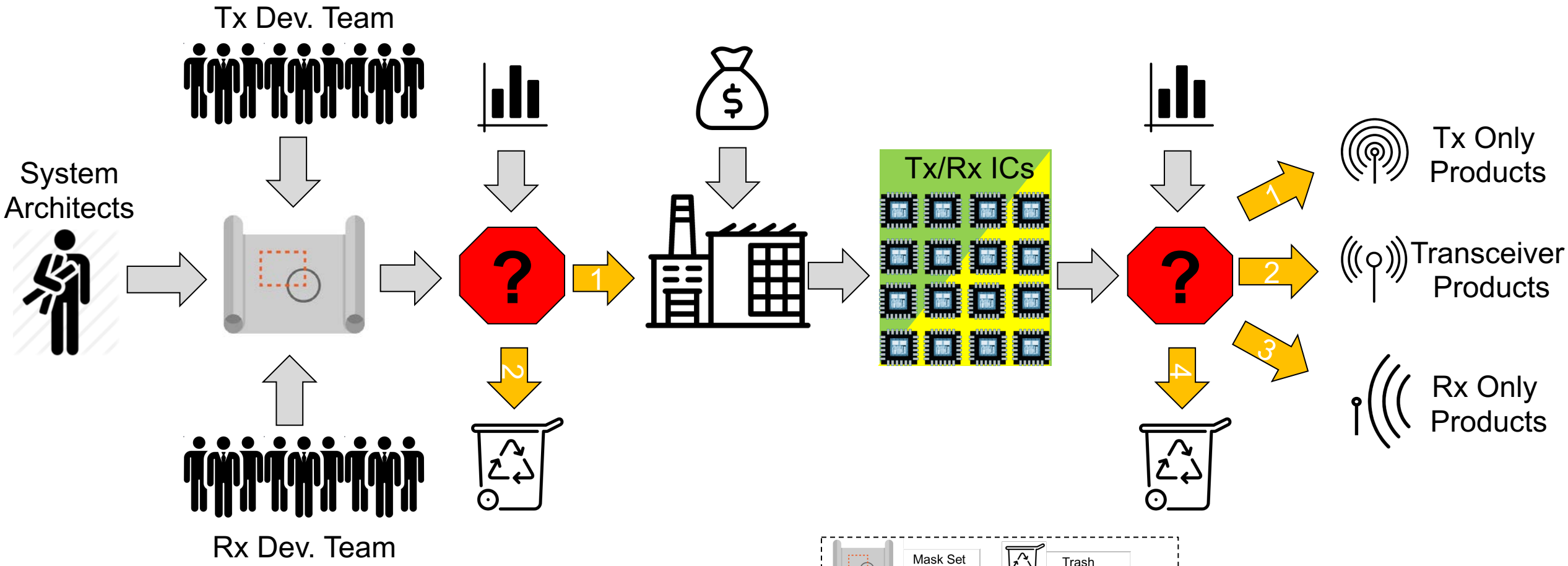


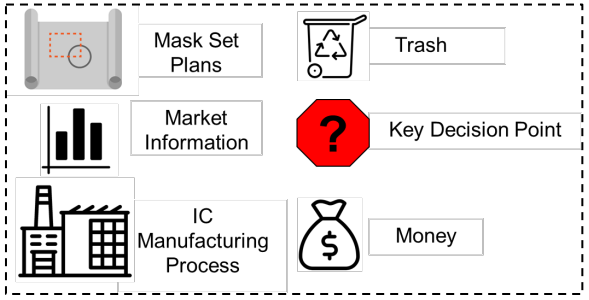
SiP Integration

Deterministic NPV = $14M

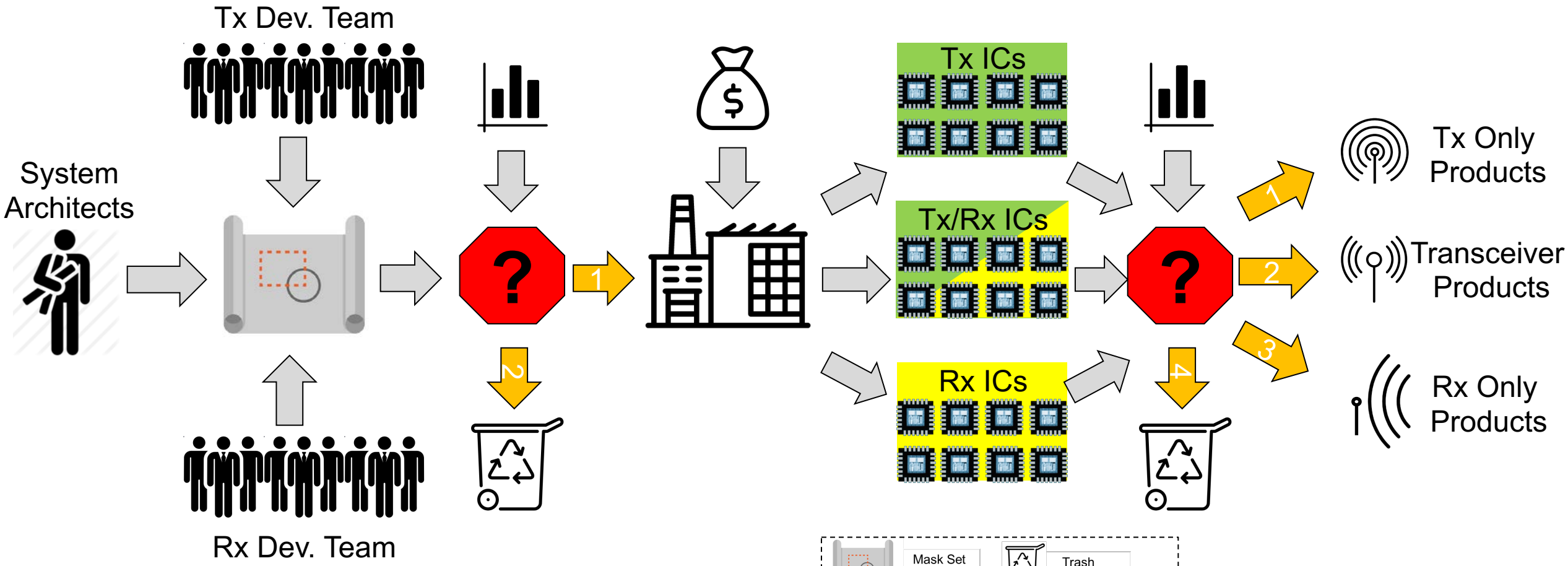


Flexible Option #1 Decision Making Process (Mono Integration)

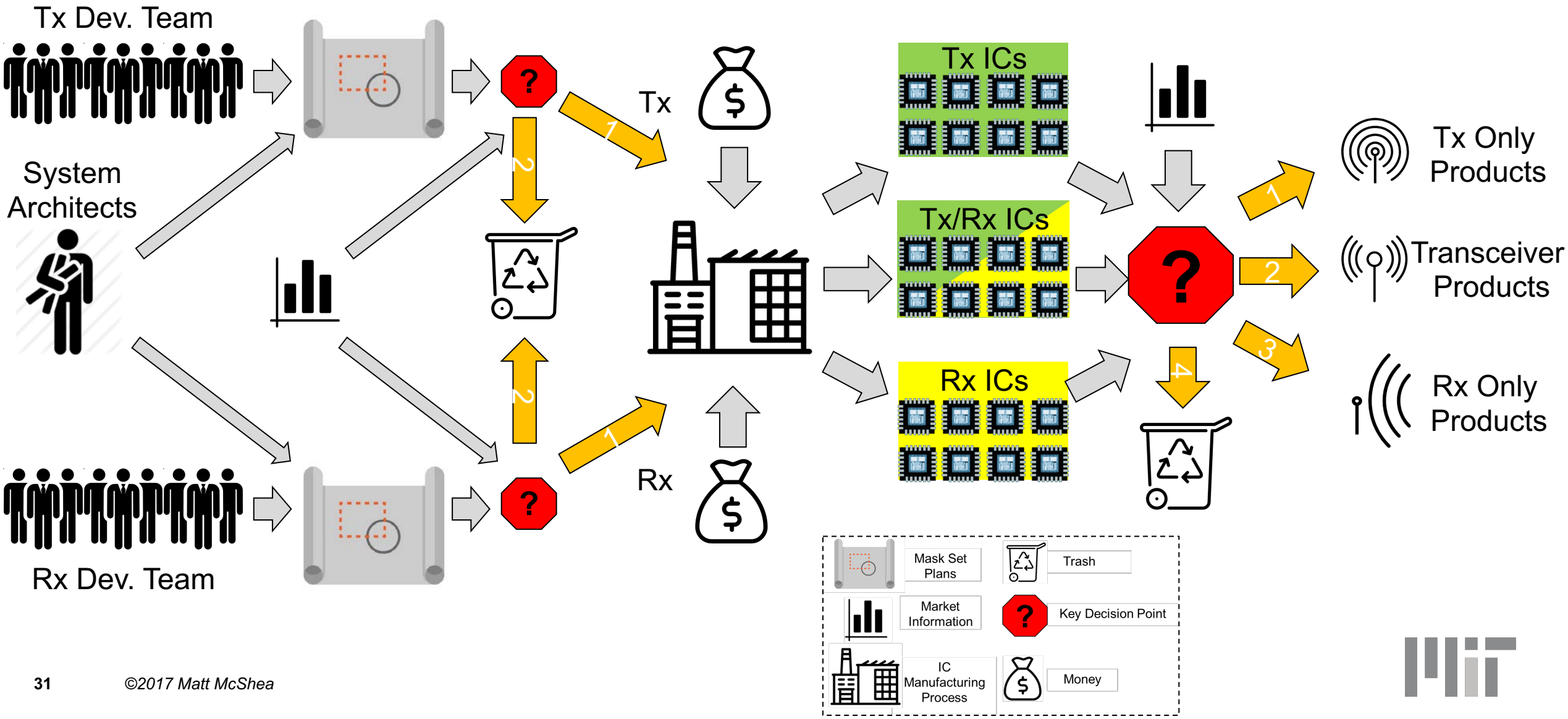




Flexible Option #2 Decision Making Process (SiP Integration)



Flexible Option #3 Decision Making Process (SiP Integration)



IDS.333 Risk and Decision Analysis

Fall 2021