## 6.012 Microelectronic Devices and Circuits Spring 2007

	March 14, 2007 Quiz #1	
		Problem #points
NAME		1
RECITATION TIME		2
		3
	Tota	al

General guidelines (please read carefully before starting):

- Make sure to write your name on the space provided above.
- Open book: you can use any material you wish. But no computers.
- All answers should be given in the space provided. Please do not turn in any extra material.
- You have 120 minutes to complete the quiz.
- Make reasonable approximations and *state them*, i.e. low-level injection, extrinsic semiconductor, quasi-neutrality, etc.
- Partial credit will be given for setting up problems without calculations. NO credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e.  $N_a,\,\tau,\,\epsilon,\,$  etc.
- Pay attention to problems in which *numerical answers* are expected. An algebraic answer will not accrue full points. Every numerical answer must have the proper *units* next to it. Points will be subtracted for answers without units or with wrong units. In situations with a defined axis, the *sign* of the result is also part of the answer.

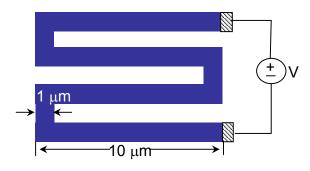
Unless otherwise stated, use:

q = 1.6 X 10<sup>-19</sup> C kT/q = 25 mV at room temperature  $n_i = 10^{10} \text{ cm}^{-3}$  for silicon at room temperature  $\varepsilon_{si} = 10^{-12} \text{ F/cm} \quad \varepsilon_{ox} = 3.45 \text{X} 10^{-13} \text{ F/cm}$ 

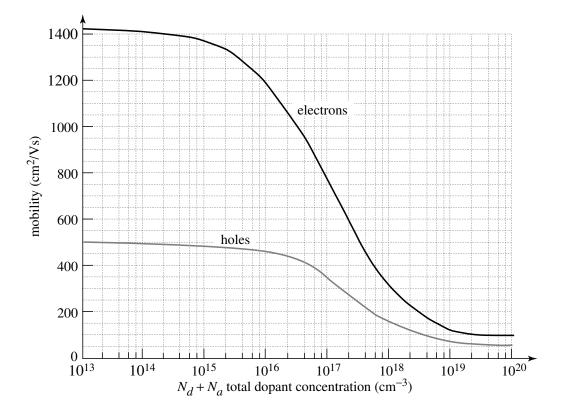
#### 1. (30 points)

The following is a serpentine IC resistor made by ion-implantation of Phosphorus into ptype Si. The repeating stripes have length of 10  $\mu$ m, and width of 1  $\mu$ m, and the connecting regions are 1x1 $\mu$ m. The dimensions are shown below. The Phosphorus dose implanted per unit area equals Q=10<sup>13</sup> cm<sup>-2</sup>, and the thickness after postannealing is t=0.1 $\mu$ m. You may ignore the contact potential effect and assume uniform doping. Please use Figure 2 below to derive mobility.

Figure 1: TOP VIEW



#### Figure 2:



(a) Compute the doping concentration in the resistor, assuming that the Phosphorus concentration is constant down to a depth of 0.1  $\mu$ m. Indicate the majority and minority carriers and calculate their concentration in thermal equilibrium at room temperature.

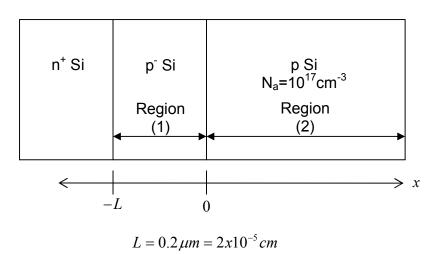
(b) Compute the total resistance of the structure.

(c) If the voltage is 1V, calculate the electric field inside one of the 10  $\mu m$  x1  $\mu m$  stripes.

- (d) In reality, the electron velocity will saturate when the electric field inside the semiconductor reaches a certain value. The saturation velocity of the majority carrier is 10<sup>7</sup> cm/s. Calculate:
  - a. The voltage when this happens,
  - b. The maximum drift current that can flow, assuming that the carriers are drifting at the saturation velocity.

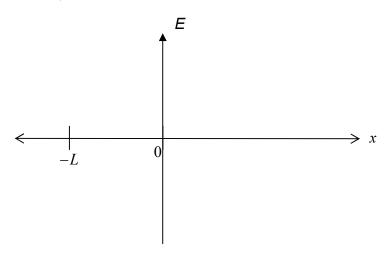
## 2. (35 points)

Consider the n<sup>+</sup> p diode shown below in thermal equilibrium. The n<sup>+</sup> doping is high enough such that you can assume that  $\phi_{n^+} = 0.55V$ , and that no potential drop occurs on the n<sup>+</sup> side of the junction. Assume that the p<sup>-</sup> Si region between x = -L and x = 0 is very lightly doped (i.e.  $N_a < 10^{15} cm^{-3}$ ).



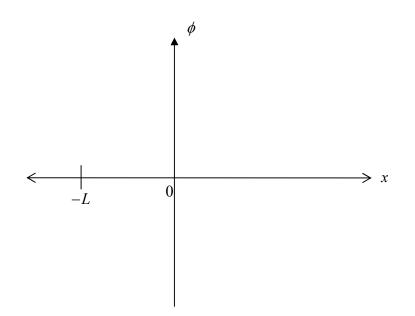
(a) Calculate the built-in potential across the structure.

(b) Sketch the electric field vs x in the structure assuming you can ignore the depletion charge in region (1). You do not need to calculate numerical values, but label the curves in the various regions with the dependence on x (e.g. linear, quadratic, etc.).



(c) Calculate the distance the depletion region extends into region (2) (i.e. beyond x = 0). (Hint: treat region (1) as a dielectric without charge)

(d) Calculate the potential drop across region (1),  $\Delta V_1$  and the potential drop across region (2),  $\Delta V_2$ , and sketch  $\phi(x)$  vs. *x* on the axes below. Label all the relevant potential drops on the sketch.

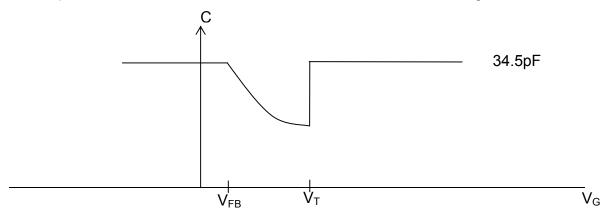


(e) Calculate the depletion capacitance of the structure at V = 0V, in units of F/cm<sup>2</sup>.

# 3. (35 points)

You are given an MOS capacitor with a  $p^+$  polysilicon gate.

The capacitor has: Area= $10^{-4}$  cm<sup>2</sup> N<sub>a</sub>= $10^{17}$  cm<sup>-3</sup> and the C-V curve given below.

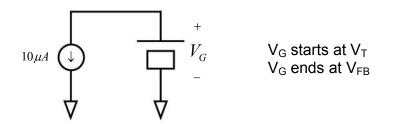


(a) Calculate the oxide thickness. Note: capacitance is given in pF not pF/cm<sup>2</sup>.

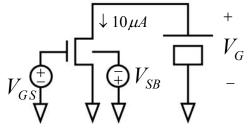
(b) Calculate the electric field in the oxide when the gate voltage equals  $V_T$ .

(c) Calculate V<sub>FB</sub>.

(d) Given a  $10\mu A$  current source is used to discharge the capacitor from V<sub>T</sub> to V<sub>FB</sub>, calculate how long it will take. Recall  $10\mu A = 10\mu C / \text{sec}$ .



(e) We replace the current source with an NMOS transistor W / L = 20 and  $V_{GS} - V_T = 0.1V$ . Calculate the mobility of the channel electrons such that the transistor drain current is  $10 \mu A$ . Assume the oxide thickness is the same as in part (a) and  $V_{SB} = 0V$  and  $\lambda = 0$ .



(f) If the transistor has a backgate voltage of  $V_{SB} = 2V$ , calculate the new gate-tosource voltage,  $V_{GS}$ , to produce the same current,  $10 \mu A$ . 6.012 Microelectronic Devices and Circuits Spring 2009

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