CMOS gates consist of an output node connected to a pull-up circuit that contains only PFETs and a pull-down circuit that contains only NFETs.

In our example, our gate computes F(A,B,C,D).

It is observed that F(1,0,1,1) = 1.

With that information, what can you say about the value of F(1,0,0,0)?

All CMOS gates are inverting which means that if all your inputs are 0, then only the PFETs in the pull-up are on, and so the output = 1.

If all your inputs are 1, then only the NFETs in the pull-down circuitry are on, and the output = 0.

If we are told that F(1,0,1,1) = 1 and we want to find out what F(1,0,0,0) is, we notice that the difference between the first set of inputs and the second is that the third and fourth inputs have been changed from 1 to 0 while the others remain unchanged.

Changing an input from 1 to 0 will turn more PFETs on, and more NFETs off, which means that there are more possibilities of the pull-up circuitry to pull the output up to high, and fewer chances of the pull-down circuitry pulling the output down to 0.

Since, we were already producing a high output with even fewer PFETs turned on, we are guaranteed that by turning more PFETs on and turning some NFETs off, the only thing we can do is maintain our high output.

So F(1,0,0,0) = 1.